



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,277	11/14/2003	Yuan-Chang Huang	681954-137US	2046
570	7590	03/28/2006	EXAMINER	
AKIN GUMP STRAUSS HAUER & FELD L.L.P.			ROSE, KIESHA L	
ONE COMMERCE SQUARE				
2005 MARKET STREET, SUITE 2200			ART UNIT	
PHILADELPHIA, PA 19103			PAPER NUMBER	
			2822	

DATE MAILED: 03/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/714,277

Applicant(s)

HUANG ET AL.

Examiner

Kiesha L. Rose

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 March 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3,5-7,9-11,13-16 and 21-34 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3,5-7,9-11,13-16 and 21-34 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____

DETAILED ACTION

This Office Action is in response to the request for reconsideration filed March 8, 2006.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-3,5-7,9-11,13-16 and 21-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon et al. (U.S. Publication 2004/0219715) in view of Farnworth et al. (U.S. Patent 6,333,555).

Kwon discloses a semiconductor device (Figs. 6 and 9) that contains a substrate (100) comprising circuits (180), a plurality of conductive bumps (220) provided in adjacent relationship to each other on substrate in electrical contact with circuits and having upper surface, pair of sidewalls, an outer wall and inner wall, a conductive layer (230/180(on top of bump Fig. 9)) made of gold (Au) provided on plurality of conductive bumps wherein conductive layer is absent from both sidewalls and inner wall, a shoulder provided in conductive layer and a protection layer (190) provided on substrate adjacent to rows of plurality of conductive bumps and a test probe pad (210 that extends on the substrate past the bump). Kwon discloses all the limitations except for

Art Unit: 2822

the conductive bump to include an electrically insulative layer. Whereas Farnworth discloses an electrically conductive bump (Fig. 1f) that contains an electrically insulating bump layer (polymer (polyimide)) (26) and a conductive layer (34) formed over electrically insulative layer. The electrically insulating bump (26) is formed to electrically engage contacts on the semiconductor components, i.e. dice, wafers, etc. (Abstract) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Kwon by incorporating an electrically insulating bump layer to electrically engage contacts on the semiconductor components, i.e. dice, wafers, etc. as taught by Farnworth. In regards to claim 27, an anisotropic conducting film (350) disposed between the first substrate (400) with conductive pads (480) and second substrate (100) for electrical connection of the bumps to the conductive pads.

Claims 1-3,5-7,9-11,13-15 and 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi (U.S. Publication 2003/0183933) in view of Farnworth.

Kobayashi discloses a semiconductor device (Figs. 3a and 19) that contains a substrate (3) comprising circuits (13), a plurality of conductive bumps (10) provided in adjacent relationship to each other on substrate in electrical contact with circuits and having upper surface, pair of sidewalls, an outer wall and inner wall, a conductive layer (1) made of gold (Au) provided on plurality of conductive bumps wherein conductive layer is absent from both sidewalls and inner wall, a protection layer (105) provided on substrate adjacent to rows of plurality of conductive bumps and a shoulder (etched area

Art Unit: 2822

of the conductive layer 1 so it does not completely cover the bump) at the upper surface of the bump. Kobayashi discloses all the limitations except for the conductive bump to include an electrically insulative layer. Whereas Farnworth discloses an electrically conductive bump (Fig. 1f) that contains an electrically insulating bump layer (polymer (polyimide)) (26) and a conductive layer (34) formed over electrically insulative layer. The electrically insulating bump (26) is formed to electrically engage contacts on the semiconductor components, i.e. dice, wafers, etc. (Abstract) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Kwon by incorporating an electrically insulating bump layer to electrically engage contacts on the semiconductor components, i.e. dice, wafers, etc. as taught by Farnworth.

Response to Arguments

Applicant's arguments with respect to claims 1-3,5-7,9-11,13-16 and 21-34 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

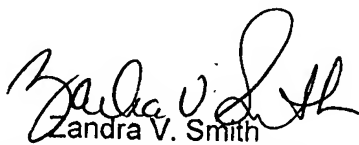
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 571-272-1844. The examiner can normally be reached on T-F 8:30-6:00 off Mondays.

Art Unit: 2822

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


KLR


Zandra V. Smith
Supervisory Patent Examiner
20 March 2006